

WHAT IS CLAIMED IS:

- 1 1. A method of computing cyclical redundancy check bits for a message
2 comprising:
3 receiving a first word of the message, the first word comprising a plurality of
4 message bits;
5 computing a plurality of feedforward bits for the first word by logically
6 combining a plurality of the plurality of message bits into a plurality of logical expressions,
7 combining the plurality of logical expressions into a plurality of terms, and storing the plurality
8 of terms as a plurality of feedforward bits;
9 providing the plurality of feedforward bits to a first logic circuit;
10 providing a plurality of cyclical redundancy check bits using the first logic circuit;
11 providing a plurality of feedback bits for the plurality of cyclical redundancy
12 check bits using a feedback circuit; and
13 providing the plurality of feedback bits to the first logic circuit.
- 1 2. The method of claim 1 wherein the first logic circuit is a summing circuit.
- 1 3. The method of claim 2 wherein the summing circuit provides an
2 exclusive-or function.
- 1 4. The method of claim 2 wherein the feedback circuit is pipelined such that
2 it receives an input and provides a corresponding output two clock cycles later.
- 1 5. A method of computing cyclical redundancy check bits for a message
2 comprising:
3 receiving a first word of the message, the first word comprising a plurality of
4 message bits;
5 computing a plurality of feedforward bits for the first word using a feedforward
6 circuit, wherein the feedforward circuit receives the first word and provides the plurality of
7 feedforward bits after N clock cycles;
8 providing the plurality of feedforward bits to a first logic circuit;
9 providing a plurality of cyclical redundancy check bits using the first logic circuit;

10 providing a plurality of feedback bits for the plurality of cyclical redundancy
11 check bits using a feedback circuit, wherein the feedback circuit receives the plurality of cyclical
12 redundancy check bits and provides the plurality of feedback bits after $2N$ clock cycles; and
13 providing the plurality of feedback bits to the first logic circuit.

1 6. The method of claim 4 wherein N is equal to one.

1 7. An integrated circuit comprising:

2 a circuit configured to receive a message and provide a plurality of cyclical
3 redundancy check bits comprising:

4 a feedforward circuit; and

5 a feedback circuit, where an output of the feedforward circuit and an
6 output of the feedback circuit are coupled to a logic circuit, wherein an output of the logic circuit
7 provides the cyclical redundancy check bits, and

8 wherein the feedforward circuit comprises a first plurality of logic gates coupled
9 to receive the message and provide outputs to a second plurality of logic gates,

10 wherein at least one of the first plurality of logic gates couple to at least two of the
11 second plurality of logic gates.

1 8. The integrated circuit of claim 7 wherein the first logic circuit is a
2 summing circuit.

1 9. The integrated circuit of claim 8 wherein the summing circuit provides an
2 exclusive-or function.

1 10. The integrated circuit of claim 9 further comprising a plurality of flip-
2 flops coupled to provide outputs to the first plurality of logic gates.

1 11. The integrated circuit of claim 9 further comprising a plurality of flip-
2 flops coupled to receive inputs from the first plurality of logic gates and provide outputs to the
3 second plurality of logic gates.

1 12. The integrated circuit of claim 9 further comprising a plurality of flip-
2 flops coupled to receive outputs from the second plurality of logic gates.

1 13. A receiver for use in data networks comprising an integrated circuit, the
2 integrated circuit comprising:
3 a first circuit configured to receive words in a data message, wherein each word is
4 a first number of bits in length;
5 a first summing node configured to receive an output from the first circuit;
6 a second circuit configured to receive an input from the first summing node and
7 provide an output to the first summing node;
8 a third circuit coupled to receive an input from the first summing node; and
9 a second summing node configured to receive an output from the first summing
10 node, an output from the third circuit, and provide a plurality of cyclical redundancy check bits.

1 14. The receiver of claim 13 wherein the first circuit left shifts each input
2 word by a second number of bits, divides the result by a generator, and provides the remainder as
3 an output.

1 15. The receiver of claim 14 wherein the second circuit left shifts each input
2 word by twice the first number of bits, divides the result by a generator, and provides the
3 remainder as an output.

1 16. The receiver of claim 15 wherein the third circuit left shifts each input
2 word by the first number of bits, divides the result by a generator, and provides the remainder as
3 an output.

1 17. The receiver of claim 16 wherein the first summing node and the second
2 summing node provide an exclusive-OR function.

1 18. The receiver of claim 16 wherein the first circuit left shifts each input
2 word by a second number of bits, divides the result by a generator, and provides the remainder as
3 an output each third number of clock cycles and the second circuit left shifts each input word by
4 twice the first number of bits, divides the result by a generator, and provides the remainder as an
5 output each fourth number of clock cycles, wherein the fourth number is twice the third number.

1 19. The receiver of claim 18 wherein the fourth number is two and the third
2 number is one.

1 20. The receiver of claim 18 wherein the first number is 32.